PATENT

Case Docket No. H-1111

In RE application of

S. KONISHI et al

Serial No.: 10/658,402

Group Art Unit:

2815

Filed: September 10, 2003

Assistant Commissioner for Patents

Examiner:

E. LEE

For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

| Washir | ngton, D.C. 20231 |
|--------|--|
| Sir: | |
| Transm | nitted herewith is an Amendment in the above-identfied application. |
| | Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted. |
| | A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed. |
| | No additional fee is required. |

The fee has been calculated as shown below:

| | (| COL. 1) | | ((| COL. 2) | (C | OL. 3) |
|---|---|---|-------|---------|-------------------------------------|----|----------------|
| | 1 | Claims emaining After mendment | | H Pr | ighest No. reviously Paid For | | esent Extra |
| Total | • | 17 | Minus | •• | 20 | - | 0 |
| Indep. | • | 2 | Minus | ••• | 3 | = | 0 |
| First Presentation of Multiple Dependent Claims | | | | | | | |

OR

OR

| SMALL ENTITY | | | |
|--------------|-------|-------------------|--|
| | Rate | Additional Fee | |
| × | 9 | \$ | |
| × | 42 | \$ | |
| + | 140 | \$ | |
| | Total | \$ | |

OTHER THAN A SMALL ENTITY

| Rate | Additional Fee |
|-------|-------------------|
| x 18 | \$ 0 |
| × 84 | \$ 0 |
| + 280 | \$ 0 |
| Total | \$ 0 |

If the entry in Col. 1 is less than the entry in Col. 2, write '0' in Col. 3.

If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 20, write '20' in this space.

If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 3, write '3' in this space.

The 'Highest Number Previously Paid For' (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

| | A che | ck in the amount of \$ | is attached in payment of: | |
|---|-------|---|--|------------------------------------|
| x | | Commissioner is hereby authorized dit any overpayment to Deposit Ac | to charge payment of the following fees count No. 50-1417. | associated with this communication |
| | х | Any filing fees under 37 CFR 1.1 | 6 for the presentation of extra claims. | |
| | x | Any patent application processing | ng fees under 37 CFR 1.17. | |
| | x | Any Extension of Time fees that | are necessary, which are betteby request | ed if necessary. |
| | • | TANGER & MALUR, P.C. al Rd., Suite 370 | By: | |

M Alexandria, Virginia 22314 (703) 684-1120

Date: November 24, 2004

Registration No.

34,663 Attorney for Applicant(s)



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 10/658,402 Conf

Confirmation No. 2241

Applicant: S. KONISHI et al.

Filed: September 10, 2003

Title: A SEMICONDUCTOR INTEGRATED

CIRCUIT DEVICE

TC/A.U.: 2815

Examiner: E. LEE

Docket No.: H-1111

Customer No.: 24956

Commissioner for Patents PO Box 1450 Alexandria VA 22313-1450

November 24, 2004

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the Restriction Requirement mailed October 26, 2004, in the above-referenced application, Applicants traverse the Restriction Requirement for the reasons set forth below. However, should the traversal fail, Applicants elect to prosecute Species I, as identified by the Examiner (FIGS. 1-12), which includes claims 1-4, 6-12 and 14-16.

Additionally, Applicants note that Claims 17-24 (24 being originally misnumberd as "23") were canceled by the Preliminary Amendment filed with the application on September

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10, 2003. Accordingly, claims 1-16 are currently pending in the application, as set forth in the listing of claims in the Preliminary Amendment.

Traversal of Restriction Requirement

At least claim 1 is believed to be generic of all the disclosed embodiments of the invention. Claim 1 is directed to:

- A semiconductor integrated circuit device, comprising:
 - a semiconductor substrate squared in plane surface;
- a plurality of pads disposed over a main surface of the semiconductor substrate along one side of the semiconductor substrate;
- a plurality of input/output cells disposed corresponding to the plural pads over the main surface of the semiconductor substrate;

an internal circuit forming section disposed over the main surface of the semiconductor substrate and inner than the plural input/output cells; and

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power supply wirings for internal circuit, for supplying potentials to the internal circuit forming section, said power supply wirings being respectively disposed inner than the plural input/output cells,

wherein the plural input/output cells include signal cells and power supply cells for internal circuit respectively,

wherein the plural pads includes signal pads
respectively disposed corresponding to the signal cells
and electrically connected the signal cells, and power
supply pads for internal circuit respectively disposed
corresponding to the power supply cells and electrically
connected to the power supply cells and the power supply
wirings, and

wherein the power supply pads are disposed closer to the power supply wirings than the signal pads.

A comparison of claim 1 with each of the Species I-VIII, as identified by the Examiner, shows that claim 1 can be fairly read on each of these embodiments, as the power supply pads are disposed closer to the power supply wiring than the

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signal pads in each embodiment. Therefore, it is asserted that at least claim 1 of the invention is generic and covers all embodiments of the invention set forth in the specification and drawings.

Accordingly, since at least claim 1 is generic for all the disclosed embodiments of FIGS. 1-25, the Restriction Requirement should be withdrawn, and examination of the claims should proceed.

The Commissioner is hereby authorized to charge any payment due to Deposit Account No. 50-1417.

Respectfully submitted,

MATTINGIY, STANSER & MALUR

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